Design and Fabrication of Microheaters for Localized Carbon Nanotube Growth

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Abstract - **This paper presents a reliable method for the growth of single-walled carbon nanotubes (SWNTs) at room temperature by using localized heating. A surface micromachining technique is used to create suspended microstructures for good thermal isolation. Pt resistors are integrated as the heating source, and the local growth temperature and electrical field can be controlled by the heater geometry and applied voltage. Growth of aligned nanotubes with diameters ranging from 1-10 nm has been demonstrated along the local E-field with a measured minimum resistance of approximately 12 kΩ. High-resolution thermal imaging was used to study the temperature distribution of the local heating.**

I. INTRODUCTION

Since their discovery in 1991 by Iijima [1], carbon nanotubes (CNTs) have drawn great interest from both academia and industry. Their superior properties are suitable for beyond-CMOS technology scaling and high-sensitivity chemical and biological sensors. Various CNT-based sensors have previously been demonstrated [2][3].

For material synthesis, chemical vapor deposition (CVD) is a widely used method that produces high-quality single-walled carbon nanotubes (SWNTs) [4][5]. CVD provides the opportunity to directly manufacture substantial quantities of individual carbon nanotubes. The location and size of the grown SWNTs can be controlled via catalyst patterning [6] and catalyst sizes [7], while the alignment can be guided by an external E-field [8]. However, the high growth temperatures (typically 800-1000°C) required by CVD prevents their integration into a mainstream CMOS platform. Although some low-temperature growth methods have recently been reported [9][10][11], compatibility with foundry CMOS processes still remains a challenge.

In this paper, we propose a post-CMOS CNT growth method that bridges the gap between CVD and CMOS in which microfabrication technology is used to create microheaters that can locally generate hot spots for SWNT synthesis while leaving surrounding areas at room temperature.

II. DEVICE DESIGN AND FABRICATION

The principle of the proposed localized heating is illustrated in Fig. 1. A thin-film bridge or cantilever with an integrated heater is created by using a surface micromachining technique. The suspended structure can be heated to a much
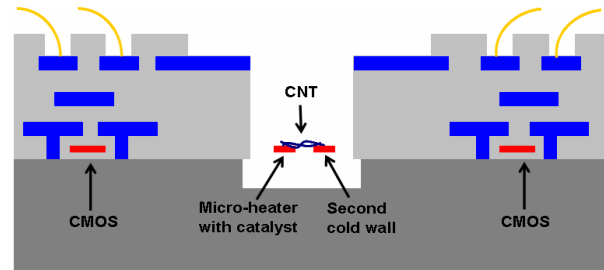

Fig.1 The concept of the CMOS integrated SWNTs.

higher temperature than the surrounding areas due to the thermal isolation of the cavity.

The maximum temperature and local temperature distribution are two critical parameters of the microheating structure. Since temperatures as high as 800°C is required for SWNT growth, thermal isolation, the resistivity of the heater, structural stiffness, and thermal stresses must be taken into consideration during design. Platinum (Pt) is chosen as the heater material since it is exceptionally stable at high temperatures. Pt is also a good temperature sensor that can facilitate real-time temperature monitoring during growth. Furthermore, Pt has been used as the contact electrode material in many traditional CVD CNT synthesis procedures [12]. The localized heating is realized by using dry etching processes to form a cavity to obtain thermal isolation. The fabrication process (shown in Fig. 2) starts from deposition of a 0.5 μm
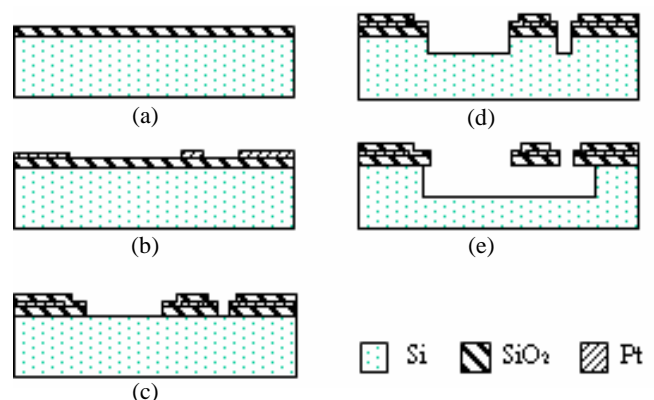

Fig.2 Fabrication process flow. (a) PECVD SiO₂ deposition. (b) Pt sputtering and lift-off to form heater and pads. (c) Top PECVD SiO₂ deposition and patterning. (d) Anisotropic Si dry etch.. (e) Isotropic Si dry etch and heater release.

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thick SiO_2. A 0.2 µm-thick Pt heater layer is sputtered and patterned using a lift-off process. Another 0.5 µm SiO_2 layer is deposited and patterned as the etching mask to release microheater hotplates (or bridges) suspended over the cavity. The SiO_2 over the microheater can be etched for direct contact between Pt and SWNTs.

Fig. 3 shows three types of microheaters that have been designed and fabricated. The first microheater design (Fig. 3a) is an 87×87 µm² micro-hotplate with a meander Pt resistor embedded, which has the potential as gas sensors. The second microheater (Fig. 3b) has a curved shape that is designed for studying E-field distribution and E-field enhancement of CNT alignment. The third microheater is further simplified into one straight line (5 µm wide and 120 µm long) (Fig. 3c) for studying temperature and SWNT density distribution along the microheater line. This will provide useful information for further scaling down to a hot spot heater. Minimization of heating elements offers accurate local control of the E-field, temperature, and growth time. Thus, the position, direction, length, quantity, and properties of SWNTs can be better controlled. Furthermore, smaller heating elements consume less power, leading to higher CNT-CMOS integration density. In the third design (Fig. 3c), two extra parallel Pt lines (on the left and right of the heater as labeled as "A" and "C", respectively) are used as the second wall for SWNT landing during growth, and as the second electrode for extracting electrical signals after synthesis. The trenches are 3 µm (left) and 6 µm (right) wide.

III. CARBON NANOTUBE GROWTH

After device fabrication, the samples are coated with an alumina/iron based catalyst by drop-drying. The large contact pads are connected to a voltage-controlled power supply by clamps, and the sample is placed into a quartz tube. After a
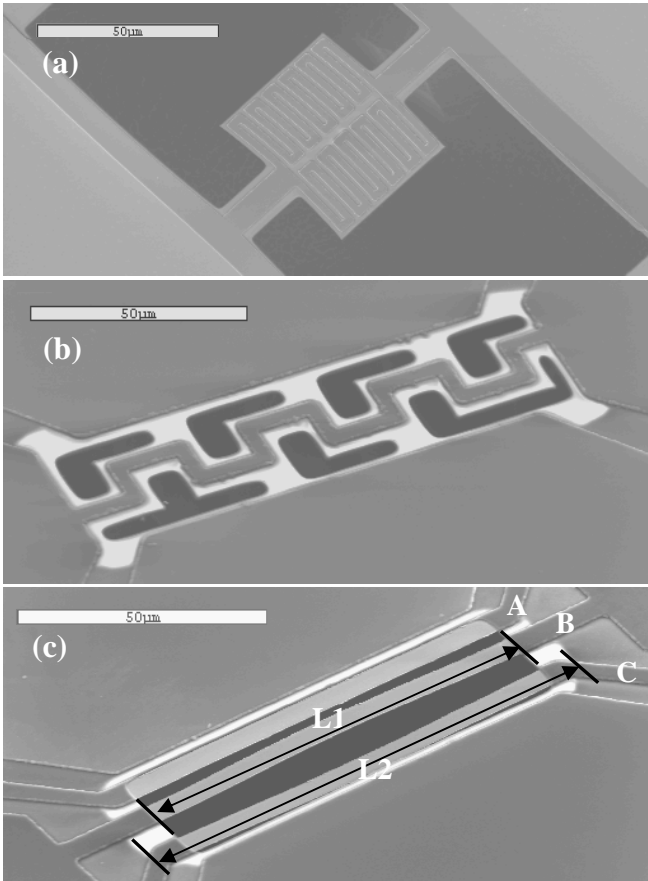
Fig.3 SEM pictures of fabricated microheaters. (a) Design-1: Pt heater embedded in a micro-hotplate, (b) Design-2: Pt heater in a curved shape, and (c) Design-3: Pt heater with two straight lines in parallel, labeled as "A", "B" and "C", respectively. L1 and L2 represent effective length of heater (80 µm) and length of cavity (about 95 µm), respectively.
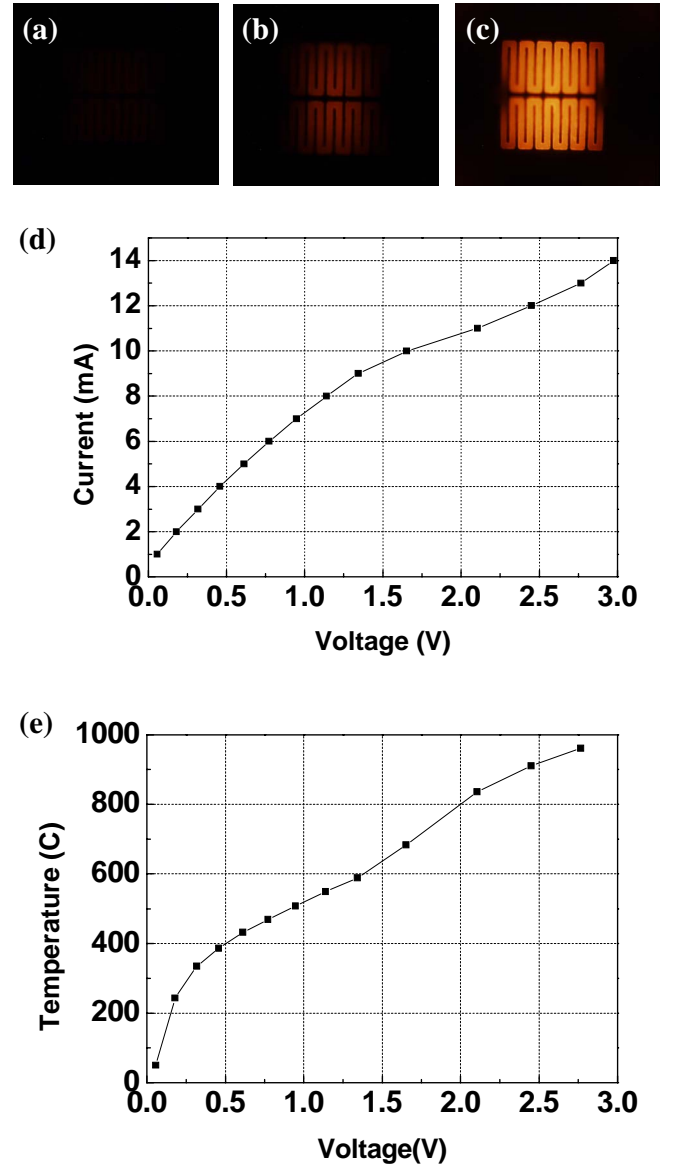
Fig.4 Thermal experiments of Design-1. (a)-(c) Microscopic photos under applied voltages of 2.28V, 2.62V and 3.0V, respectively. (d) Experimental microheater I-V data. (e) Temperature estimated based on resistivity change.
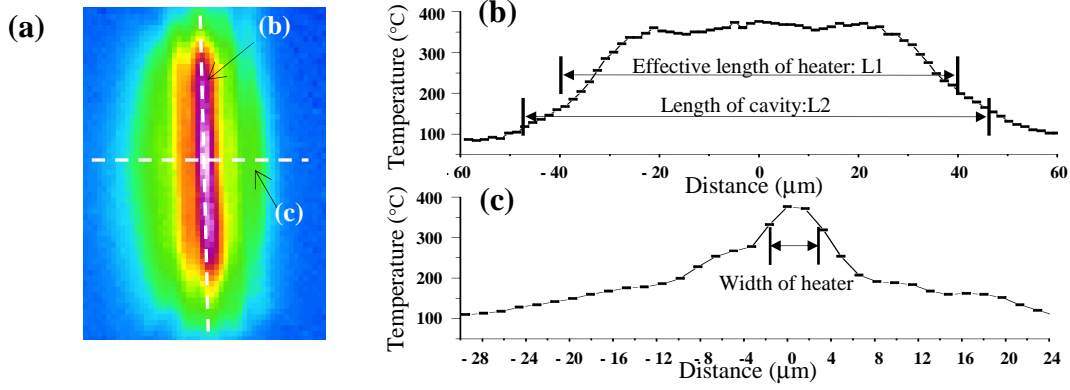
Fig.5 Thermal imaging of Design-3. (a): Thermal image by applying 0.6Vdc voltage. (b), (c): Corresponding temperature distribution along and transverse to the microheater, indicating good thermal isolation. (The substrate temperature is 60°C).

5-minute argon purge, the on-chip microheater is heated up and a mix of 1000-sccm CH_4, 20-sccm C_2H_4 and 500-sccm H_2 is flowed into the quartz tube for SWNT growth.

IV. EXPERIMENTAL RESULTS

A. Temperature characterization

First, the experimental current-voltage relationship was measured (shown in Fig. 4(d)). The maximum temperature was estimated to be over 900 °C (shown in Fig. 4(e)) based on the change of resistance and the temperature coefficient of resistance (TCR) of Pt. During the I-V characterization, red glowing of the microheater under different applied voltages was clearly observed under an optical microscope (Fig. 4(a)-(c)). This red glowing can be switched instantaneously between "on" and "off" by controlling the voltage supply, indicating much shorter response time compared to conventional CVD processes. Fast response combined with localized microheating greatly reduces the total thermal budget of post-CMOS processing.

Temperature distribution was investigated using a QFI InfraScope. Fig. 5(a) shows a thermal image of Design-3. As the working temperature range of this infrared imager is limited to 400°C, only 0.6V was applied to the microheater. The temperature distributions along and transverse to the microheater line are plotted in Fig. 5(b) and (c), respectively. The temperature is near uniform at the region ±30 µm from center point, which is the area suitable for nanotube growth. It is also clearly shown that with the temperature as high as 400°C at the heater center the temperature outside the micro cavity drops quickly to about 100°C (note that the InfraScope stage was heated to 60°C to facilitate accurate temperature measurement). Therefore the temperature is compatible with post-CMOS processing even when the voltage must be increased to provide a desired growth temperature of ~900°C. By accurately choosing the spacing between microheaters and CMOS circuits, this localized microheating method can fabricate SWNTs at a close proximity of CMOS devices on the same chip.

B. Carbon nanotubes characterization

After a 15-minute growth, SWNTs and MWNTs with diameters ranging from 1-10 nm were successfully obtained on suspended microstructures. Fig. 6 shows a dense film of SWNTs grown on the micro-hotplate surface. The orientations of these nanotubes are random since there is no ordered electrical field. On the other hand, the supply voltage introduces a uniform electrical field (about 0.1 ~ 1.0 V/ µm) between the microheater and a nearby cold ground electrode. As shown in Fig. 7(a) and (b), most of the suspended SWNTs grew on microheaters for Design-2 and Design-3, illustrating a significant alignment along the E-field perpendicular to the cold wall.

The growth of SWNTs is uniform along the length of the entire microheater (Design-3), except on regions nearest to the anchors. This coincides agreeably with the measured temperature distribution. Therefore, microheater geometry with either a relatively large hot-plate or a minimized hot-spot can be customized to control temperature distributions for regulating the quantity of SWNTs for various applications.

In the third design, three parallel Pt lines (the one in the center is a microheater) are initially separated and have no SiO_2
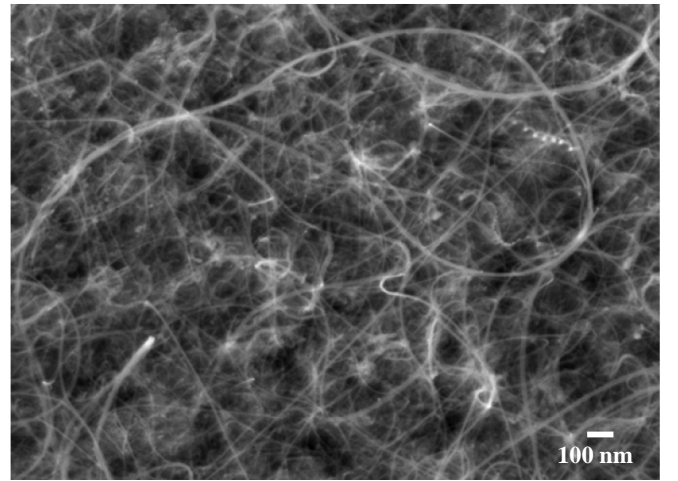

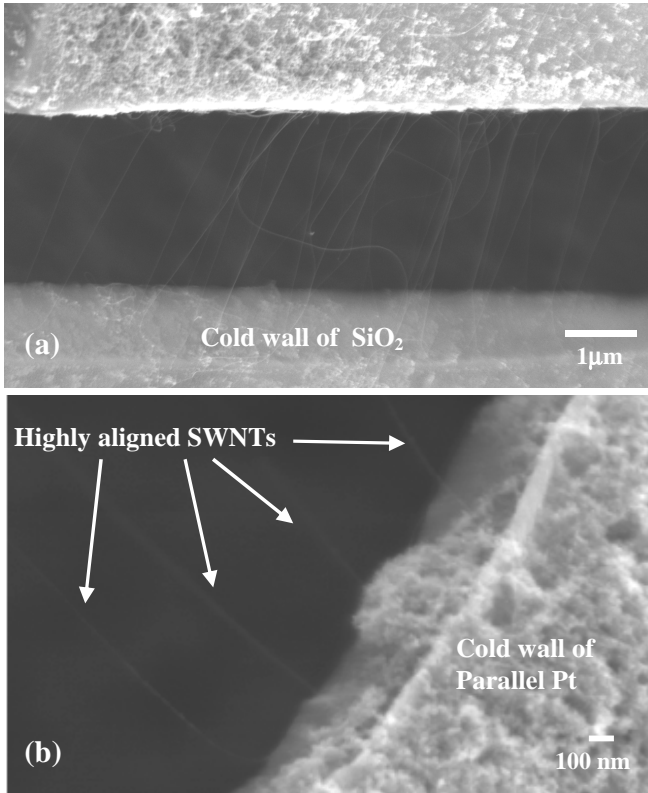Fig. 6 Dense film of Carbon Nanotubes over micro-hotplate surface.

Fig. 7   Localized synthesis of Carbon Nanotubes suspended across the trench ((a) Design-2, (b) Design-3), showing good CNT alignment.

coverage. After growth, I-V characterizations between pads A and B, B and C, and A and C are performed on the same device shown in Fig. 7(b) and then plotted in Fig. 8 (A, B and C are as labeled in Fig. 3(c)). The resistance R_{B-C} between the pads B and C (6 µm wide trench) is about 85 kΩ, while the resistance R_{B-A} between the pads B and A (3 µm wide trench) is about 12 kΩ due to the denser and shorter SWNT connection. Since nanotubes did not grow from the cold wall Pt lines, there is no direct connection between A and C. The measured resistance R_{A-C} between the pads A and C is near 100 kΩ, close to the sum of the two series-connected resistors R_{B-C} and R_{B-A}.

V.   CONCLUSION AND FUTURE WORK

Room-temperature localized chemical vapor deposition synthesis of single-walled carbon nanotubes based on three microheaters has been successfully demonstrated. Local temperature distribution has been investigated by using high-resolution thermal imaging and later confirmed by the SWNT growth density. Voltage-controlled localized heating allows the integration of SWNTs with foundry CMOS circuits. System integration combining CMOS circuits and microheaters using foundry CMOS processing is currently ongoing. Microheater scaling and optimization, E-field and temperature manipulation, investigation of other electrode materials, and specific characterization of individual SWNTs by electrical gating will be explored in the near future.
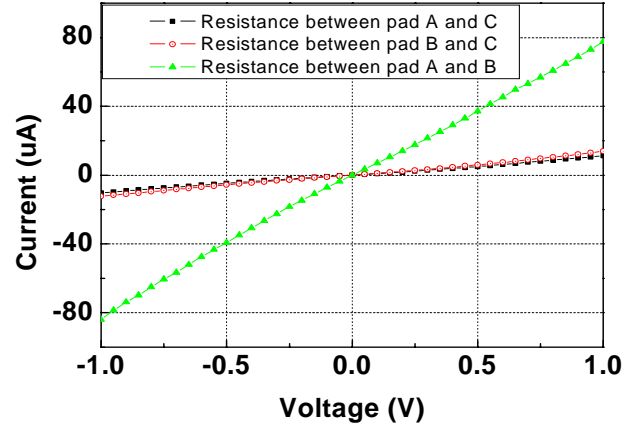

Fig.8 I-V characteristics of SWNTs contacted by Pt electrode. It was measured on the same device shown in Fig. 7(b)

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